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- 1. **The changing face of technology in distributed systems**  
Verissimo, P.; Vogels, W.;  
Distributed Computing Systems, 1993., Proceedings of the Fourth Workshop o  
of  
22-24 Sept. 1993 Page(s):119 - 127  
Digital Object Identifier 10.1109/FTDCS.1993.344167  
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- 2. **A parallel execution model for a database machine with high performance**  
Donsez, D.; Faudemay, P.;  
Databases in Parallel and Distributed Systems, 1990, Proceedings. Second Int'l  
Symposium on  
2-4 July 1990 Page(s):56 - 70  
Digital Object Identifier 10.1109/DPDS.1990.113698  
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Publisher: ACM Press

Full text available:  [pdf\(1.03 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**2 Microsoft memory management document** April 1981 **ACM SIGPC Notes**, Volume 4 Issue 1-2

Publisher: ACM Press

Full text available:  [pdf\(607.05 KB\)](#) Additional Information: [full citation](#), [abstract](#)

Memory management requirements are not unique to the XENIX system. A memory management system is required by all modern multi-user operating systems. Current mainframe and minicomputers have memory management hardware of some kind. Modern 16-bit microprocessors powerful enough to do the work of a minicomputer need similar memory management facilities.

**3 Performance and dependability evaluation of scalable massively parallel computer** [systems with conjoint simulation](#)

Axel Hein, Mario Dal Cin

October 1998 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 8 Issue 4

Publisher: ACM Press

Full text available:  [pdf\(501.59 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Computer systems are becoming more and more a part of our daily life; business and industry rely on their service, and the health of human beings depends on their correct functioning. Computer systems used for critical tasks have to be carefully designed and tested during the early design stage, the prototype phase, and their operational life. Methods and tools are required to support and facilitate this vital task. In this article, we tackle the issue of system-level performance and depen ...

**Keywords:** fault-tolerant and large-scale computer systems, hierarchical model design, object-oriented modeling, process-based simulation, timed Petri nets

**4 A hardware implementation of capability-based addressing**

 G. J. Myers, B. R. S. Buckingham  
October 1980 **ACM SIGOPS Operating Systems Review**, Volume 14 Issue 4

Publisher: ACM Press

Full text available:  pdf(1.03 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

The SWARD architecture, an experimental higher-level architecture, contains the naming and protection concept of capability-based addressing. After discussing the merits of capability-based addressing, its general representation in the SWARD architecture is discussed. The initial representation of capability-based addressing in the architecture led to a set of problems; these problems are described, as well as their solutions. Finally, the implementation of capabilities by the processor is discu ...

**5 A hardware implementation of capability-based addressing**

 G. J. Myers, B. R. S. Buckingham  
October 1980 **ACM SIGARCH Computer Architecture News**, Volume 8 Issue 6

Publisher: ACM Press

Full text available:  pdf(880.47 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

The SWARD architecture, an experimental higher-level architecture, contains the naming and protection concept of capability-based addressing. After discussing the merits of capability-based addressing, its general representation in the SWARD architecture is discussed. The initial representation of capability-based addressing in the architecture led to a set of problems; these problems are described, as well as their solutions. Finally, the implementation of capabilities by the processor is discu ...

**6 A multikey hashing scheme using predicate trees**

 Patrick Valduriez, Yann Viemont  
June 1984 **ACM SIGMOD Record , Proceedings of the 1984 ACM SIGMOD international conference on Management of data SIGMOD '84**, Volume 14 Issue 2

Publisher: ACM Press

Full text available:  pdf(815.03 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

A new method for multikey access suitable for dynamic files is proposed that transforms multiple key values into a logical address This method is based on a new structure, called predicate tree, that represents the function applied to several keys A predicate tree permits to specify in a unified way various hashing schemes by allowing for different definitions of predicates A logical address qualifies a space partition of a file according to its predicate tree This address is seen as a single ke ...

**7 Memory management units for microcomputer operating systems**

 I Rattan  
January 1987 **ACM SIGOPS Operating Systems Review**, Volume 21 Issue 1

Publisher: ACM Press

Full text available:  pdf(393.34 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Recently, independent memory management units for microprocessor based systems have become available. This note summarizes the features of register and tree memory management units (using MC68451 & MC68851 as examples) from a viewpoint of microcomputer operating systems design.

**8 On a general property of memory mapping tables**

 Karl Reed  
March 1982 **ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News ,**

**Proceedings of the first international symposium on Architectural support for programming languages and operating systems ASPLOS-I,**  
 Volume 17 , 10 Issue 4 , 2

**Publisher:** ACM Press

Full text available:  pdf(368.16 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The paper shows that memory mapping tables can be used to implement the display registers used in providing architectural support for block-structured languages such as Algol 60. This allows full lexical level addressing to be implemented on so-called von-Neuman machines. The problems of fragmentation of the paged address space are explored, and machines with memory mapping schemes capable of supporting the proposals identified. Attention is drawn to the similarity bet ...

**Keywords:** Display, Memory mapping, Page tables, Segmentation, Virtual memory

**9 Structure of an efficient duplex memory for processing fault-tolerant programs** 

 K. H. Kim, C. V. Ramamoorthy

April 1978 **Proceedings of the 5th annual symposium on Computer architecture**

**Publisher:** ACM Press

Full text available:  pdf(757.93 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Fault-tolerant programs contain redundancy to provide tolerance for residual program errors and hardware faults during task execution. The concept of parallel execution of fault-tolerant programs, i.e., overlapping main-stream computation with redundant computation related to validation and recovery, was developed in [8]. A memory scheme, referred to as "duplex memory", was also designed to realize the full potential of parallel execution. Although the duplex memory sketched in ...

**10 Storage concepts in a software-reliability-directed computer architecture** 

 Glenford J. Myers

April 1978 **Proceedings of the 5th annual symposium on Computer architecture**

**Publisher:** ACM Press

Full text available:  pdf(513.49 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Because of the tremendous difficulty of producing reliable software (application and system software) and the serious consequences of software errors, a new solution is being explored: the development of a new computer architecture that will substantially enhance the reliability of the programs executing above it. This paper concentrates on the storage concepts (e.g., data representations and addressing) in the architecture.

**11 Searching in a dynamic memory with fast sequential access** 

 Om Vikas, V. Rajaraman

July 1982 **Communications of the ACM**, Volume 25 Issue 7

**Publisher:** ACM Press

Full text available:  pdf(492.43 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This communication presents an algorithm for searching in the Aho-Ullman dynamic memory consisting of  $(2m - 1)$  cells. Mean search time of  $1.5m$  steps to the first specified record is obtained with a subsequent sequential access capability. Thus, in such a dynamic memory, the mean access time for content addressing is the same as the mean access time for random addressing.

**Keywords:** content addressing, dynamic memory, shuffle transformation

**12 Group communication in multichannel networks with staircase interconnection topologies**

P. K. McKinley, J. W. S. Liu

August 1989 **ACM SIGCOMM Computer Communication Review , Symposium proceedings on Communications architectures & protocols SIGCOMM '89**, Volume 19 Issue 4

Publisher: ACM Press

Full text available:  pdf(1.25 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Recently, multichannel networks composed of several parallel, medium-speed channels multiplexed on a single high-speed medium have been proposed as a practical way to harness the high bandwidths of optical fibers. In order to limit the cost of network interfaces, a partially-connected multichannel network allows each node access to only a proper subset of the channels, its channel set. Staircase interconnection topologies constitute a family of partially-connected multichannel networks in w ...

**13 VM/4: ACOS-4 virtual machine architecture**

S. Nanba, N. Ohno, H. Kubo, H. Morisue, T. Ohshima, H. Yamagishi

June 1985 **ACM SIGARCH Computer Architecture News , Proceedings of the 12th annual international symposium on Computer architecture ISCA '85**, Volume 13 Issue 3

Publisher: IEEE Computer Society Press, ACM Press

Full text available:  pdf(767.68 KB) Additional Information: [full citation](#), [index terms](#)

**14 A parallel execution model for a database machine with high performances**

Didier Donsez, Pascal Faudemay

July 1990 **Proceedings of the second international symposium on Databases in parallel and distributed systems**

Publisher: ACM Press

Full text available:  pdf(1.47 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper, we present a mixed MIMD / SIMD execution model for a reconfigurable computer. This model is adapted to the use of a specialized associative coprocessor, embedded in this host machine. A main characteristic of the model is that it uses four types of processes (decoding, calculus, coprocessor communication and transaction manager), and that in principle one process of each type is allowed on each processor. Time intervals are allocated to operations into partitions of t ...

**15 Order-preserving key transformations**

Anil K. Garg, C. C. Gotlieb

June 1986 **ACM Transactions on Database Systems (TODS)**, Volume 11 Issue 2

Publisher: ACM Press

Full text available:  pdf(1.22 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

File organizations based on conventional hash functions provide faster access to the stored records in comparison with tree-like file structures. Tree structures such as B+-trees and ISAM do provide for sequential processing, but require considerable storage for the indices. When sequential processing is needed a table that performs an order-preserving transformation on keys can be used. H is an order-preserving key transform if  $H(K_1) \leq H(K_2)$  whenever  $K_1 \leq K_2$ .

**16 IFIP WG2.1 Subcommittee: Data Processing and Transput**

Peter Naur

March 1972 **ALGOL Bulletin**, Issue 33

**Publisher:** Computer History Museum

Full text available:  pdf(895.15 KB) Additional Information: [full citation](#), [index terms](#)

**17 The evolution of the Sperry Univac 1100 series: a history, analysis, and projection** 

 B. R. Borgerson, M. L. Hanson, P. A. Hartley

January 1978 **Communications of the ACM**, Volume 21 Issue 1

**Publisher:** ACM Press

Full text available:  pdf(1.89 MB) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

The 1100 series systems are Sperry Univac's large-scale mainframe computer systems. Beginning with the 1107 in 1962, the 1100 series has progressed through a succession of eight compatible computer models to the latest system, the 1100/80, introduced in 1977. The 1100 series hardware architecture is based on a 36-bit word, ones complement structure which obtains one operand from storage and one from a high-speed register, or two operands from high-speed registers. The 1100 Operating System ...

**Keywords:** 1100 computer series, computer architecture, data management systems, end user facilities, executive control software, multiprocessing, multiprogramming, operating system, programming languages

**18 A dynamic hash method with signature** 

 F. Cesarini, G. Soda

May 1991 **ACM Transactions on Database Systems (TODS)**, Volume 16 Issue 2

**Publisher:** ACM Press

Full text available:  pdf(1.54 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#), [review](#)

We present a dynamic external hash method that allows retrieval of a record by only one access to mass storage while maintaining a high load factor. The hash function is based on generalized spiral storage. Both primary and overflow records are allocated to the same file, and file expansion depends on being able to allocate every overflow chain to one bucket. An in-core index, built by means of a signature function, discriminates between primary and overflow records and assures one access to ...

**Keywords:** dynamic hashing, external hashing, generalized spiral storage, signature functions

**19 Firmware structure and architectural support for monitors, vertical migration and user microprogramming** 

Mamoru Maekawa, Ken Sakamura, Chiaki Ishikawa

March 1982 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices , Proceedings of the first international symposium on Architectural support for programming languages and operating systems ASPLOS-I**, Volume 10 , 17 Issue 2 , 4

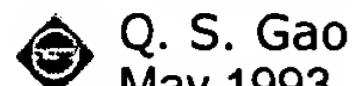
**Publisher:** ACM Press

Full text available:  pdf(754.07 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper describes firmware and hardware support necessary for constructing easy-to-understand and high performance operating systems including language translators and interpreters. Basic principles are one-to-one correspondence between logical hierarchy and physical hierarchy, and vertical migration. Implementation of monitors in firmware and architectural support for it are discussed, and a sample system is shown.

Architectural support for user microprogramming is then discussed and an ...

20 The Chinese remainder theorem and the prime memory system



Q. S. Gao  
May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture ISCA '93**, Volume 21 Issue 2

Publisher: ACM Press

Full text available: [pdf\(287.10 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

As we know, the conflict problem is a very important problem in memory system of super computer, there are two kinds of conflict-free memory system approaches: skewing scheme approach and prime memory system approach. Previously published prime memory approaches are complex or wasting  $1/p$  of the memory space for filling the "holes" [17], where  $p$  is the number of memory modules. In this paper, based on Chinese remainder theorem, we present a perfect prime memory system which only ...

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